**Experiment / Assignment / Tutorial No. 4**

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of the Staff In-charge with date**

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| **Batch: B1 Roll No.: 1711072 Experiment / assignment / tutorial No.: 4** |

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| **Title:** 4 bit Magnitude Comparator |

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**Objective:** Design a 2-bit comparator using logic gates and verify 4-bit magnitude comparator using IC 7485

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**Expected Outcome of Experiment:**

**CO2:** Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

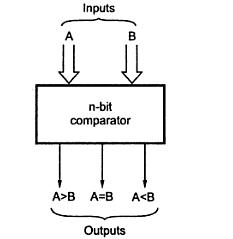
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**Books/ Journals/ Websites referred:**

* R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill
* M .Morris Mano, “Digital Logic & computer Design”, PHI
* http://elnsite.teilam.gr/ebooks/digital\_design/lab/dataSheets\_page/7485.pdf

**Pre Lab/ Prior Concepts:**

The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B, A=B (or) A<B.



**Two Bit Magnitude Comparator Implementation Details:**

**Truth Table**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **A1** | **A0** | **B1** | **B0** | **A > B** | **A = B** | **A < B** |
|  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 |  |  |  |  |  |  |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
|  |  |  |  | 0 |  |  |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
|  |  |  |  |  |  |  |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
|  |  |  |  |  |  | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
|  |  |  |  |  |  |  |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
|  |  |  |  |  |  | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
|  |  |  |  |  |  |  |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
|  |  |  |  |  |  |  |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
|  |  |  |  |  |  |  |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
|  |  |  | 0 |  |  |  |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
|  |  | 1 |  |  |  |  |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
|  |  |  |  |  |  |  |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
|  |  |  |  |  |  |  |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
|  |  |  |  |  |  |  |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
|  |  |  |  |  |  |  |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |
|  |  |  |  |  |  |  |

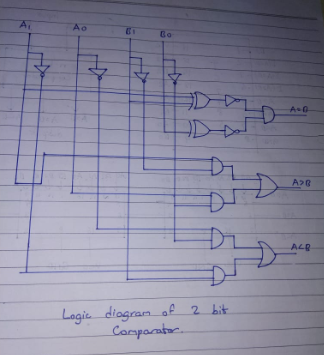
**From the Truth Table:**

**(A<B)= A1’A0’B0+A1’B1+A0’B1B0**

**(A=B)= (A1 B1)(A0B0)**

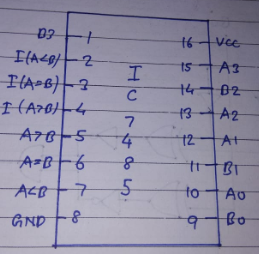
**(A>B)= AoB1’B0’+A1A0B0’+A1B1’**

**Logic Diagram of 2 bit Comparator**

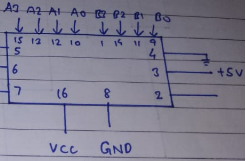


**Four Bit Magnitude Comparator Implementation Details**

**Pin Diagram of IC 7485**



**Logic Diagram of IC 7485**



**Comparing Table**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Comparing inputs | | | | | | | | Cascading inputs | | | Outputs | | |
| A3 | B3 | A2 | B2 | A1 | B1 | A0 | B0 | A>B | A<B | A=B | A>B | A<B | A=B |
| A3>B3  A3<B3  A3=B3  A3=B3  A3=B3  A3=B3  A3=B3  A3=B3  A3=B3  A3=B3  A3=B3  A3=B3  A3=B3  A3=B3 | | X  X  A2>B2  A2<B2  A2=B2  A2=B2  A2=B2  A2=B2  A2=B2  A2=B2  A2=B2  A2=B2  A2=B2  A2=B2 | | X  X  X  X  A1>B1  A1<B1  A1=B1  A1=B1  A1=B1  A1=B1  A1=B1  A1=B1  A1=B1  A1=B1 | | X  X  X  X  X  X  A0>B0  A0<B0  A0=B0  A0=B0  A0=B0  A0=B0  A0=B0  A0=B0 | | X | X | X | 1 | 0 | 0 |
| X | X | X | 0 | 1 | 0 |
| X | X | X | 1 | 0 | 0 |
| X | X | X | 0 | 1 | 0 |
| X | X | X | 1 | 0 | 0 |
| X | X | X | 0 | 1 | 0 |
| X | X | X | 1 | 0 | 0 |
| X | X | X | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| X | X | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 |

**Conclusion:**

1-bit and 2-bit comparators were successfully designed using gates, whereas 4-bit comparator was verified successfully using IC 7485. We also learned that cascading can be done using (C 7485 for designing higher bits comparators like 8-bit and so on.

**Post Lab Descriptive Questions**

1. Design a 1- bit magnitude comparator using logic gates.

Ans.

